

UNIT 1

Fundamentals of Microprocessor

(5 Hours) — Microprocessor and Computer Architecture (CACS155)

1. Introduction to Microprocessors

A microprocessor is a program-controlled semiconductor device (fabricated on a single Integrated Circuit chip) that fetches, decodes and executes instructions to perform arithmetic, logical, control and data-transfer operations. It forms the "brain" of a digital computer system — it does not, by itself, store data or programs permanently; instead it works together with memory and input/output devices to form a complete computer system.

- It is a multipurpose, programmable, clock-driven, register-based electronic device.
- It reads binary instructions from memory, decodes them, and executes the corresponding operation.
- It communicates with memory and I/O devices through address, data and control buses.
- Its capability is measured in terms of word length (8-bit, 16-bit, 32-bit, 64-bit), clock speed, and instruction set.

1.1 Evolution of Microprocessors

Generation	Example	Word Size	Key Feature
1st (1971–73)	Intel 4004, 8008	4-bit / 8-bit	PMOS technology, very limited instruction set
2nd (1973–78)	Intel 8085, Motorola 6800, Zilog Z80	8-bit	NMOS technology, richer instruction set
3rd (1978–80)	Intel 8086/8088, Motorola 68000	16-bit	HMOS technology, pipelining introduced
4th (1980–85)	Intel 80386	32-bit	Multitasking, virtual memory support
5th (onwards)	Pentium, Core i-series	32/64-bit	Superscalar, multi-core, pipelined architecture

1.2 Basic Functional Block Diagram

Every microprocessor, irrespective of its generation, is built around three fundamental units working together: the Arithmetic and Logic Unit (ALU) which performs computations, the Control Unit which generates timing and control signals, and the Register Array which provides fast, temporary internal storage. These units communicate internally and externally through a common set of buses, described next.

2. Microprocessor Systems with Bus Organization

A microprocessor never works in isolation — it forms the CPU of a larger microprocessor-based (or microcomputer) system, which additionally requires memory to hold programs and data, and input/output devices to communicate with the outside world. These three sub-systems are interconnected by a common pathway called a bus.

A bus is a group of conducting wires which carries information, all peripherals are connected to a microprocessor through a bus. There are three types of buses in a typical microprocessor system:

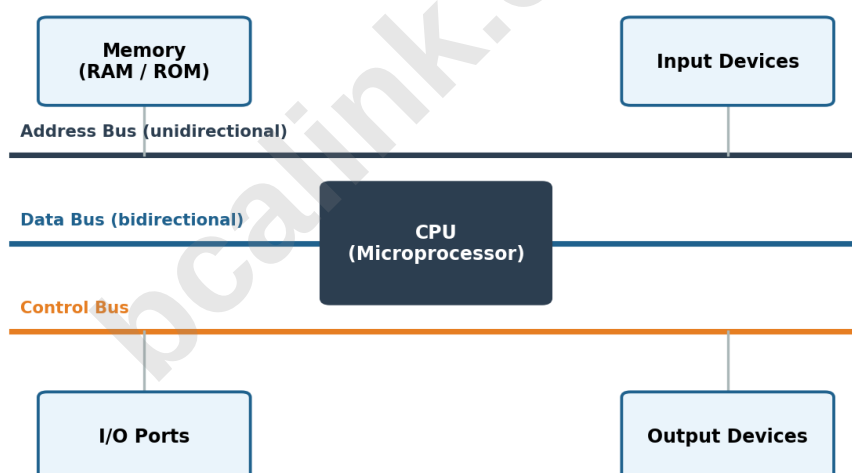


Figure 1.1 — Bus organization of a microprocessor-based system

Bus	Direction	Purpose
Address Bus	Unidirectional (CPU → Memory/IO)	Carries the address of the memory location or I/O port to be accessed. Its width (number of lines) decides the maximum addressable memory — an n-bit address bus can address 2^n locations.
Data Bus	Bidirectional (CPU ↔ Memory/IO)	Carries the actual data or instruction code being transferred. Its width decides the word length of the microprocessor (8085 has an 8-bit data bus).

Bus	Direction	Purpose
Control Bus	Bidirectional (individual lines mostly unidirectional)	Carries timing and control signals such as Read (RD), Write (WR), Memory/IO select, Reset, Interrupt requests, etc., to synchronise all operations.

Note: An n -bit address bus can access 2^n distinct memory locations. For example, the 8085 has a 16-bit address bus, so it can address $2^{16} = 65,536$ (64 KB) memory locations.

Example 1.1

A microprocessor has 20 address lines and 16 data lines. Determine (a) the maximum memory it can address, and (b) the word length of the data it can transfer at once.

Solution

(a) Maximum memory locations = $2^{20} = 1,048,576 = 1 \text{ MB}$

(b) Since the data bus is 16 bits wide, the microprocessor transfers 16 bits (2 bytes) of data in one bus cycle.

3. Microprocessor Architecture and Operation

Internally, a microprocessor is organised into several functional blocks that cooperate to fetch, decode and execute instructions. The generic internal architecture (irrespective of the specific chip) consists of the following units:

Unit	Function
Arithmetic & Logic Unit (ALU)	Performs arithmetic operations (add, subtract) and logical operations (AND, OR, XOR, complement, shift/rotate).
Accumulator	A special register that holds one of the operands before an ALU operation and receives the result after it.
General Purpose Registers	Provide fast on-chip storage for data and addresses, reducing the need for slower memory access.
Program Counter (PC)	Holds the address of the next instruction to be fetched from memory; it is automatically incremented after every fetch.
Stack Pointer (SP)	Holds the address of the top of the stack, a reserved area of memory used for temporary storage (e.g., during subroutine calls).
Instruction Register & Decoder	Holds the fetched instruction (opcode) and decodes it to determine the operation to be performed.
Timing and Control Unit	Generates the sequence of control and timing signals needed to fetch, decode and execute each instruction.

Unit	Function
Flag Register	A set of flip-flops (Sign, Zero, Carry, Parity, Auxiliary Carry, etc.) that record the status of the result of the last ALU operation.

3.1 Basic Operation Cycle

Regardless of the instruction being executed, a microprocessor repeatedly performs the same basic cycle:

- **Fetch** — The address in the Program Counter is placed on the address bus; the instruction (opcode) stored at that address is read from memory into the Instruction Register, and PC is incremented.
- **Decode** — The Instruction Decoder interprets the opcode to determine what operation is to be performed and which operands/registers are involved.
- **Execute** — The Control Unit generates the necessary control signals, and the ALU (or other unit) carries out the operation; results are stored back in a register or memory.

Note: This Fetch–Decode–Execute sequence is repeated continuously for every instruction in a program and is the foundation of the stored-program computer concept.

4. The 8085 Microprocessor and Its Operation

The Intel 8085 is an 8-bit, NMOS microprocessor introduced by Intel in 1976. It has an 8-bit data bus, a 16-bit address bus, operates on a single +5V power supply, and requires an external clock (typically generated using a crystal, often 6 MHz, internally divided by 2 to give an operating frequency of up to 3 MHz).

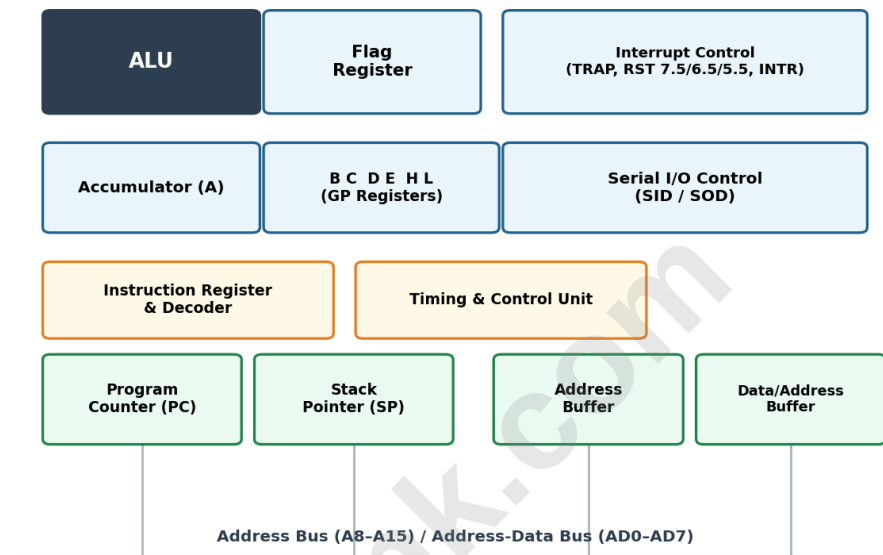


Figure 1.2 — Internal architecture of the 8085 microprocessor

4.1 Register Organization

Register	Size	Description
Accumulator (A)	8-bit	Primary register for arithmetic/logic operations; holds one operand and the result.
B, C, D, E, H, L	8-bit each	General-purpose registers; can be paired as BC, DE, HL for 16-bit operations.
Flag Register (F)	8-bit (5 flags used)	Holds S (Sign), Z (Zero), AC (Auxiliary Carry), P (Parity), CY (Carry) flags.
Program Counter (PC)	16-bit	Points to the address of the next instruction to be fetched.
Stack Pointer (SP)	16-bit	Points to the top of the stack in read/write memory.
Instruction Register (IR)	8-bit	Temporarily holds the fetched opcode (not programmer-accessible).

4.2 Key 8085 Pins and Signals

- ALE (Address Latch Enable) — demultiplexes the AD0–AD7 lines into separate address and data lines during the first clock cycle of a machine cycle.
- RD / WR — active-low control signals indicating a memory/I/O read or write operation.
- IO/M — distinguishes whether the current operation is a memory access or an I/O access.
- READY — used by slow peripherals to insert wait states and synchronise with the CPU.
- HOLD / HLDA — used for Direct Memory Access (DMA) operations.
- INTR, RST 7.5, RST 6.5, RST 5.5, TRAP — five hardware interrupt inputs (TRAP has the highest priority and is non-maskable).
- SID / SOD — serial input data and serial output data lines for simple serial communication.

5. Instruction Cycle, Machine Cycle and T-States

The execution of every instruction in the 8085 is broken down hierarchically into three timing concepts:

Term	Definition
T-state (Clock Period)	The smallest unit of time; one T-state equals one clock cycle of the input clock signal.
Machine Cycle	The time required to complete one operation of accessing memory or an I/O device (e.g., Opcode Fetch, Memory Read, Memory Write, I/O Read, I/O Write). One machine cycle consists of 3 to 6 T-states.
Instruction Cycle	The total time required to fetch and execute one complete instruction. It consists of one to six machine cycles, depending on the instruction.

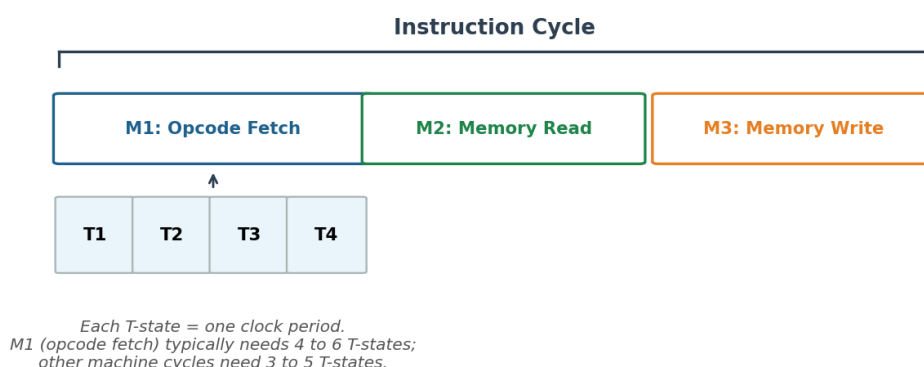


Figure 1.3 — Relationship between instruction cycle, machine cycles and T-states

Every instruction cycle begins with the Opcode Fetch (M1) machine cycle, which needs a minimum of 4 T-states (extended to 6 T-states for certain instructions). Subsequent machine

cycles such as Memory Read, Memory Write, I/O Read and I/O Write typically require 3 T-states each (I/O operations may need an additional wait state since the 8085 always inserts one wait state during I/O machine cycles).

Example 1.2

The instruction **MVI A, 32H** (Move Immediate) requires one Opcode Fetch machine cycle (4 T-states) followed by one Memory Read machine cycle (3 T-states) to fetch the 8-bit immediate data. Calculate the total number of T-states and the execution time if the clock frequency is 3 MHz.

Solution

Total T-states = 4 (M1: Opcode Fetch) + 3 (M2: Memory Read) = 7 T-states

Clock period $T = 1 / 3 \text{ MHz} = 0.333 \mu\text{s}$

Execution time = $7 \times 0.333 \mu\text{s} \approx 2.33 \mu\text{s}$

6. Addressing Modes in 8085

An addressing mode defines the way in which the operand of an instruction is specified/accessed. The 8085 supports five addressing modes:

Addressing Mode	Description	Example
Immediate	The operand (data) is specified directly within the instruction itself.	MVI A, 32H
Register	The operand is held in one of the internal CPU registers.	MOV A, B
Direct	The 16-bit address of the operand is specified directly in the instruction.	LDA 2050H
Indirect (Register Indirect)	The address of the operand is held in a register pair (usually H-L), which points to memory.	MOV A, M
Implied (Implicit)	The operand is implied by the opcode itself; no operand needs to be specified.	CMA, RAL, STC

Note: In Register Indirect addressing, the H-L register pair conventionally acts as a memory pointer; the operand denoted by 'M' actually refers to the memory byte at the address held in HL.

7. Introduction to the 8086 Microprocessor

The Intel 8086, introduced in 1978, is a 16-bit microprocessor and the first member of the x86 family that still influences processor design today. It significantly advanced upon the 8085 in word size, addressing capability and internal architecture.

Feature	8085	8086
Data bus width	8-bit	16-bit
Address bus width	16-bit	20-bit
Maximum addressable memory	64 KB	1 MB
Internal architecture	Single unit (no pipelining)	Two units — Bus Interface Unit (BIU) and Execution Unit (EU), enabling pipelining
Number of registers	6 general 8-bit registers	8 general 16-bit registers plus segment registers
Memory organization	Flat (linear) addressing	Segmented memory addressing (CS, DS, SS, ES)

A key architectural innovation of the 8086 is the division of the CPU into two independent, concurrently-operating units:

- Bus Interface Unit (BIU) — responsible for fetching instructions from memory, reading/writing data, and address calculation using segment registers; it maintains a 6-byte instruction queue (prefetch queue).
- Execution Unit (EU) — decodes and executes instructions fetched by the BIU, and contains the ALU, general-purpose registers and flag register.

Because the BIU can fetch the next instruction(s) into its queue while the EU is still executing the current instruction, the 8086 achieves a simple two-stage pipelining effect, which improves overall throughput compared to the purely sequential fetch–decode–execute cycle of the 8085.

Key Takeaways

- ✓ A microprocessor is the programmable CPU of a computer system, built around an ALU, control unit and register array.
- ✓ A microprocessor-based system communicates via three buses: Address (unidirectional), Data (bidirectional) and Control.
- ✓ An n-bit address bus can address 2^n memory locations; the data bus width determines the microprocessor's word length.
- ✓ The 8085 is an 8-bit microprocessor with a 16-bit address bus (64 KB addressable memory) and a 5-stage register set including A, B, C, D, E, H, L.
- ✓ Every instruction executes as an Instruction Cycle made up of Machine Cycles, each made up of T-states (clock periods).
- ✓ The 8085 supports five addressing modes: Immediate, Register, Direct, Indirect and Implied.
- ✓ The 8086 extended the architecture to 16-bit data, 20-bit addressing (1 MB memory), segmented memory, and introduced pipelining via separate BIU and EU units.

— *End of Unit 1* —